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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,536	10/31/2001	Pradeep Sindhu	1014-014US01	4412

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EXAMINER

AVELLINO, JOSEPH E

ART UNIT	PAPER NUMBER
2143	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/004,536

Applicant(s)

SINDHU ET AL.

Examiner

Joseph E. Avellino

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-35 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-35 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2002/02/22
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-35 are presented for examination; claims 1, 9, 18, 24, 30, and 35 independent.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9, and 12-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugai et al. (USPN 6,671,277) (hereinafter Sugai).

3. Referring to independent claims 1 and 9 (e.g. exemplary claim 1), Sugai discloses a routing component (e.g. routing processor, or RP) comprising:

a first interface to communicate with a first network interface (Figure 1, ref. 30);

a second interface to communicate with a second network interface (Figure 1, ref. 20, 30); and

an embedded memory 11 to buffer data communicated from the first interface to the second interface (Figure 2, ref. 11, 12).

4. Referring to claim 4, Sugai discloses the first interface comprises a WAN interface (Figure 2; col. 4, lines 22-31).
5. Referring to claim 5, Sugai discloses the second interface comprises a switch fabric interface (i.e. crossbar switch) (Figure 1, ref. 20).
6. Referring to claim 6, Sugai discloses the switch fabric interface communicates crossbar data (Figure 1, ref. 20; col. 5, lines 36-47)
7. Referring to claim 7, Sugai discloses the routing component is implemented using an ASIC (it is understood in the art and in the specification as defined on page 4, an ASIC is a circuit board or chip which is designed for a particular function, in this case the routing component 12 is integrated on a single silicon chip, therefore it is implemented as an Application Specific IC, the Application in this case is to provide routing function) (Figure ; col. 4, lines 18-32).
8. Referring to claim 8, Rowett discloses the embedded memory comprises a RAM (Figure 1, ref. 22).

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9. Claims 12-17 are rejected for similar reasons as stated above. Furthermore Sugai discloses comprising a second router having an embedded memory to store data communicated using the second network interface (Figure 1, ref. 10).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2, 3, 10, 11, and 18-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugai in view of Ernil et al. (USPN 6,745,246) (Hereinafter Ernil).

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12. Referring to claim 2, Sugai discloses the invention substantively as described in claim 1. Sugai does not specifically disclose comprising an interface to an external memory for buffering data communicated from the second interface to the first interface. In analogous art, Erimil discloses another routing component system which includes an interface to an external memory for buffering data communicated from the second interface to the first interface (col. 6, lines 1-5). It would be obvious to a person of ordinary skill in the art at the time the invention was made to combine the teaching of Erimil with Sugai since Sugai discloses requiring two memory read/write steps (one in the receiving RP for the incoming packet data, and then this data is written in the output RP to be transmitted on the second port) which is well known in the art to be very expensive overhead in processor architecture. The external buffer system of Erimil reduces this memory processing in half by only writing the packet in once and reading the packet once, thereby reducing overall computer processing overhead and increasing router throughput.

13. Referring to claim 3, Sugai in view of Erimil disclose the system substantively as described in claim 2. Sugai in view of Erimil do not specifically disclose the external memory has a greater storage capacity than the embedded memory, however it is well known that external memory (i.e. hard drives, flash drives, etc.) can have a higher storage capacity than embedded memory such as registers and Random Access Memory. Therefore it would have been obvious to assume the external memory would

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have a greater storage capacity than the embedded memory since it would allow for more packets to be stored and thereby reducing page faults in the external device.

14. Claims 10, 11, and 18-35 are rejected for similar reasons as stated above.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

16. Rowett et al. (USPN 6,366,583) discloses a network router integrated on a single chip.

17. Gentry et al. (USPN 5,778,180) discloses reducing data copying in protected memory OS.

18. Torudlbakken et al. (USPN 6,633,580) discloses an NxN crossbar packet switch.

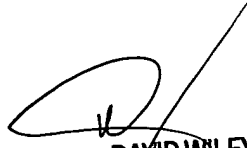
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph E. Avellino whose telephone number is (571) 272-3905. The examiner can normally be reached on Monday-Friday 7:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEA
December 14, 2004



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